Comprehensive Assessment of FinFET Technology for Extending Moore's Law to Nanoscale Devices

Mohit Shukla*, Pawan Srivastava*, Ram Chandra Singh Chauhan**

* MTech, Microelectronics, Institute of Engineering and Technology, Lucknow, India -226021.

** Associate Professor, ECE Department, Institute of Engineering and Technology, Lucknow, India -226021.

***Abstract*-** Downscaling has been the constant need of the hour for the past two decades to realize low power, high speed and high-density devices. Until higher technology nodes came into the scene, the planar CMOS structures were offering better performance but the limitations started setting in with the progression towards lower nodes. In order to resolve this obstacle, FinFET based devices were proposed as they possess multiple Gate structure resulting in better control over the channel region and hence, charge carriers. This paper discusses the limitations of planar CMOS technology which paved the way for the advent of FinFETs. A literature review of the studies carried out on FinFETs in the past twenty years have also been presented along with a comparative analysis on FinFET based SRAM circuits.

***Index Terms*-** short channel effects, FinFET, CMOS, scaling, SRAM

I. INTRODUCTION

Gordon Moore predicted that the number of transistors present on the same area of integrated chip would increase by a factor of two every 18 months [1], [2]. This process is also referred by the terms 'down scaling' or 'miniaturization'. Reduction in minimum feature length of transistors governs this phenomenon. It provides designers with the capability to place more transistors on the same chip area. Integrated circuit chip designers employ miniaturization technique as it equips the devices with higher speed, lower power and higher packing density. The transistors become smaller in size and interconnects become shorter. This leads to reduction in capacitance (equation 1) which in turn decreases the circuit delay (equation 2) as the speed at each node increases by 30 percent [3].

$$C = \frac{\varepsilon * A}{d} \quad \text{- (1)}$$

$$\tau = \frac{C * V}{I} \quad \text{- (2)}$$

Here, in equation 1, C is capacitance, $\boldsymbol{\varepsilon}$ is permittivity of material used in transistor, A is area of chip, d is separation between individual devices on chip. In equation 2, $\boldsymbol{\tau}$ is propagation delay, V is the supply voltage and I denote the drive current. According to rule of thumb, the shrinking of device dimension leads to 30 percent decrement in previous width and previous height, each, which cumulates to the new area being 0.49 times of the reduction in area. This can be explained with equation 3 and 4.

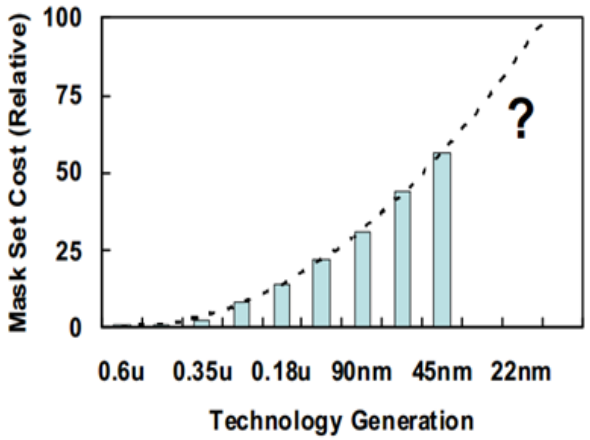

Fig.1. Relation of mask set cost with technology node **[2]**

$$New\ area = (0.7 * previous\ height) * (0.7 * previous\ width) \quad \text{- (3)}$$

$$New\ area = (0.49 * previous\ area) \quad \text{- (4)}$$

Downscaling comes with benefits in the form of higher speed, lower power consumption and higher density of transistors on the integrated circuit chip but it also puts forth many challenges when we shrink the technology node beyond a certain limit, typically below 32nm technology node. As the channel length is decreased, the Source/Drain-depletion regions enter the channel area. The close proximity of these two depletion regions can result in quantum- mechanical tunneling of electrons from Source to Drain. The shrinking of Gate-oxide layer could lead to electrons tunneling from channel to Gate. Other obstacles include effects such as hot carrier effect, Drain Induced Barrier Lowering (DIBL),

surface scattering of carriers, sub threshold leakage, threshold voltage reduction. The aforementioned effects are referred to as the Short Channel Effects (SCE). A number of noise sources are also observed for instance ground noise, leakage noise, substrate noise as a reason for reduced control over the channel due to downscaling process.

Another perspective of this phenomenon involves increasing the transistor integration capacity which also increments design complexity resulting in elevation of design and validation costs. With technology miniaturization, cost of transistors goes down by half whereas on the other hand, the cost of fabrication facilities and mask sees a rise [4]. Scaling down of MOS transistors leads to lowering of device performance and high leakage resulting in increased consumption of power, interconnect delay, noises and parasitic capacitances. Some research articles have reported downscaling to be the cause of reduction in Gate controllability on charges traversing in the channel region. This is one of the causes for the occurrence of SCE [5].

Due to the fact that CMOS technology approaches a lot of limitations as we proceed towards lower technology nodes, there was a need for new device structures, especially below 32nm. Multigate FETs, commonly known as FinFETs, emerged out as an alternative to the planar MOS transistors as they offer excellent control over channel. The rest of the paper comprises of following sections: section II presents introduction of FinFETs, section III reviews few research papers on FinFETs. Comparative analysis of FinFET based SRAM research works has been covered in section IV. We explore the challenges of FinFET devices in section V and section VI concludes the paper.

II. INTRODUCTION TO FINFETS

FinFET was first proposed by Chenming Hu and his colleagues in University of California at Berkeley in 1990s. However, it is worth noting that idea of multigate transistors was first conceptualized in 1987 by Hieda et al [6]. The structure of FinFETs can be visualized similar to the MOS transistor rotated by 90 degrees along the Drain-Source, thus, forming a wrapped-like structure as shown in figure 2. Planar MOSFETs have horizontal channel whereas vertical channel is present in FinFETs. The Gate of FinFET is wrapped around the channel in order to provide better control over the charge transport occurring in the channel. The short channel effects caused due to the threshold variations were overcome by employing multigate devices. They possess a non-planar structure and are being capable of being operated in different modes such as low-power, independent gate and shorted gate [7]. FinFETs have higher ON current and high device scalability.

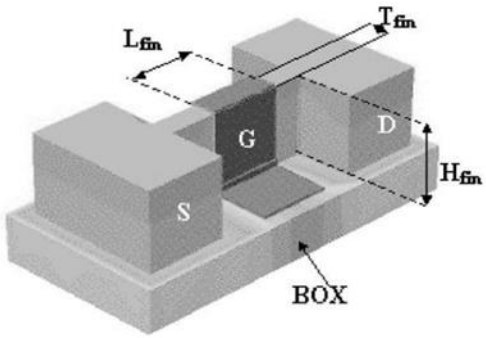

Fig.2. FinFET basic structure [8]

The main issue faced while scaling of devices takes place is the leakage current during off-state. FinFET is able to annihilate the short channel effects to a satisfactory limit added with high current driving ability [9]. The FinFET technology is an emerging pillar in this era which possesses low power consumption, requiring small area, robustness against short channel effects and faster operational speed. They are said to be quasi-planar since the direction of current is parallel to wafer and channel is perpendicular to the current direction flow [10]. The reason for the name "Fin" FET is due to the fact that the Source and Drain of the structure resemble the fins of fish. Fins are the most important and crucial part of FinFETs. Stability of FinFETs is defined by the fin height. Small fins render more stability to the structure as they make it more flexible, when compared with the long fin counterpart [11], [12].

Channel length in FinFET is associated to fin height referred to as width optimization. Hence, current flow in the ON state can be incremented by increasing fin height and number of fins [11]. The quantum confinement effects causes an increase in the threshold voltage as we decrement the fin width [13]. One of the obstacles while down scaling the MOS transistors was the loss of controllability over the channel charge. This issue could be resolved by increasing number of Gates of transistor which increases the capability of Gate to control channel charge [14], [15]. This idea is employed by multigate transistors. Fin height is a quantifiable factor. It is restricted in the sense that there can only be integral number of fins in a FinFET. By accumulating number of fins, we can get improved electrostatic control over the channel current. Channel length of FinFET device is given by the equation 5.

$$L\_ch = 2 * (H\_fin) + T\_fin \quad -(5)$$

Here, L_ch is the length of channel, T_fin is the thickness of fin and H_fin is the height of fin. Initially, FinFET structure was presented as Silicon-on-Insulator (SoI) type. In this classification, the fins (that is Drain and Source regions) are isolated from the Silicon substrate due to presence of SiO_2 in between. SoI FinFETs have the capability of suppressing any possible leakage that might occur between Source and Drain. It also boasts high speed characteristic due to low values of Drain/Source to Substrate capacitance.

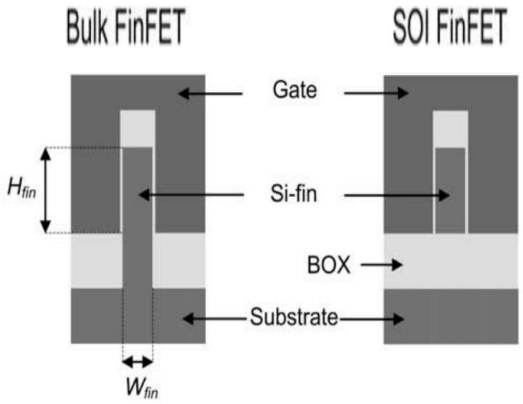

Fig.3. SOI and Bulk FinFET [16]

The bulk-FinFET structure has garnered recognition lately due to its high compatibility with the planar CMOS structure. It has an added advantage of low fabrication cost incurred. The fins of bulk-FinFET structure are etched out all the way through SiO_2 to make contact with the Silicon substrates, thus making it stand apart from the SoI counterpart. Owing to its unique structure, the bulk-FinFETs have an exorbitant rate of heat transfer to the substrate.

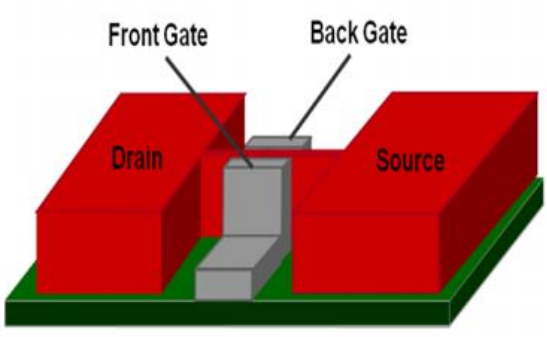

Fig.4. Independent Gate (IG) FinFET [17]

FinFETs can be classified into two additional categories based on the connection of Gate terminal, namely Independent Gate (IG) and Shorted Gate (SG). IG FinFETs have four-terminals comprising of two separate gates, making it a four-terminal device [18]. In this, the designer has the liberty of being able to apply two different signals at the two gates giving a higher electrostatic control over the channel charge. The only disadvantage is requirement of more fabrication area which elevates the cost.

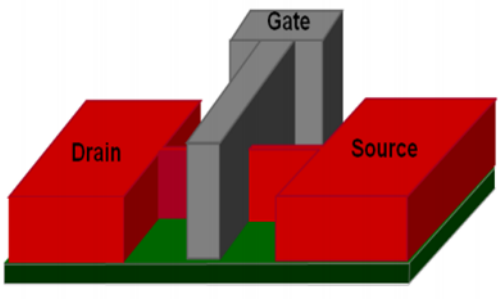

Fig.5. Shorted Gate (SG) FinFET [17]

The other class of FinFETs is referred to as Shorted-Gate FinFETs. In this, the two gates (as in case of IG FinFETs) are connected together, thus making it a three-terminal device. The off-state current in SG FinFETs is higher than that in case of IG FinFETs. Due to the gates being shorted, only one signal can be applied at the (shorted) gate terminal [19].

III. LITERATURE REVIEW

A rigorous research study has been carried out on FinFETs for over two decades, resulting in thousands of publications. Some of these include studying of the impact intensity of short channel effects on FinFETs, heat tolerance, impact of dopants on the device and deriving new fault models for circuits. With the limitations of planar CMOS technology staring at our face now, the semiconductor industry researchers are considering the FinFET technology to substitute CMOS. This section explores some of the previous research publications on FinFETs.

A) "**Fault Modeling for FinFET Circuits**" by Muzaffer O Simsir et al., 2010 [20]

- This work discusses whether the fault models of CMOS technology are sufficient and capable enough to model all the defects of FinFETs.

- Here the authors examined the behavior of inverter and NAND logic gates by deliberately introducing defects, shorting each transistor's Source and Drain terminals.
- Results exhibited a need to introduce new fault models in order to capture all defects in FinFETs.

B) "**Impact of Parameter Variations on FinFET Faults**" by G. Harutyunyan et al., 2015 [21]

- In this paper, the authors presented a compact analysis concerned with effects of parameter variations on the faults observed in FinFET based memories.
- Three FinFET based memory instances and two FinFET models, namely fin-open and gate-fin short, were chosen to carry out this study.

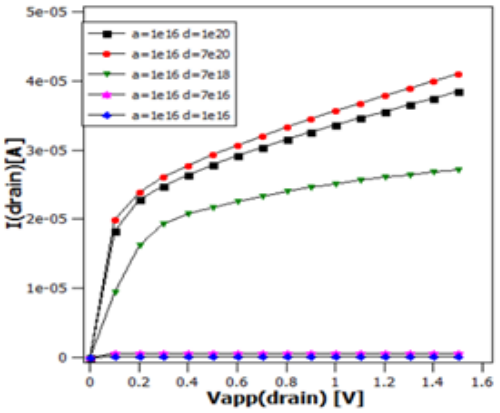

Fig.6. I_d –V_d curve for 32nm Gate length n-FinFET [22]

C) "**32nm Gate length FinFET: Importance of Doping"** by Neha Somra and RS Sawhney, 2015 [22]

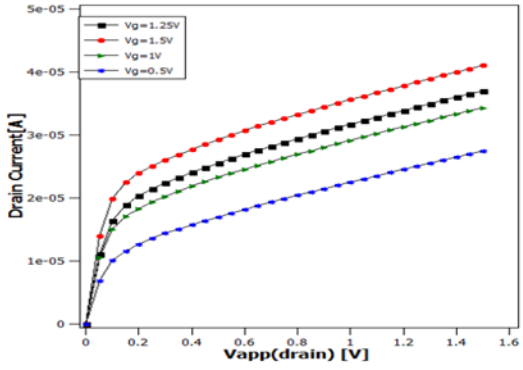

Fig.7. I_d increase with increasing drain/ source impurity [22]

- This paper explores the impact of doping on FinFETs.
- Implementation of circuits was done with the help of TCAD software.
- It was inferred from the results that Drain current increases with increase in Gate voltage, which deduced that resistance decreased at higher Gate voltage.

D) "**Low Leakage Current Symmetrical Dual-k 7 nm Trigate Bulk Underlap FinFET for Ultra Low Power Applications**" by Mahmud S. Badran et al., 2017 [23]

- This work was concerned with achieving lowest possible leakage current for ultra-low-power applications.
- Implementation of proposed FinFET was carried out using Sentaurus TCAD software and attempted to decimate leakage current by making adjustments in spacer length, subthreshold effective length and work function.
- Results proved that the proposed FinFET circuit achieved lowest leakage current compared to the publications till that year.

E) "**Investigation of Electrothermal behaviors of 5nm Bulk FinFET"** by Jongmook Jeon et al., 2017 [24]

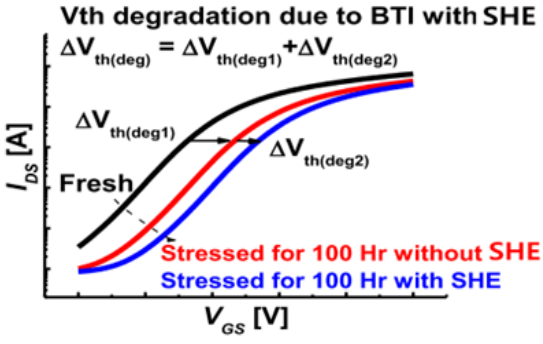

Fig.8. Variation of I_{DS} versus V_{GS} demonstrating the self-heating effect [24]

- This work was concerned with self-heating effect (SHE) in bulk FinFETs. The reliability and performance of FinFET devices are badly affected by SHE.

- In technology nodes as low as 5nm, generally heat gets dissipated via metal interconnects instead of substrate, thus, giving rise to self-heating of the structure. It occurs due to poor thermal coupling between fins and the substrate.

- The authors also proposed a new Figure of Merit (FoM) given by

$$FoM = \frac{1}{(\tau d)*(\Delta Vth\_degrad)} \quad \text{- (6)}$$

τd is inverter propagation delay and ΔVth_degrad is degradation of threshold voltage due to negative bias temperature instability (NBTI) owing to variations in device dimensions.

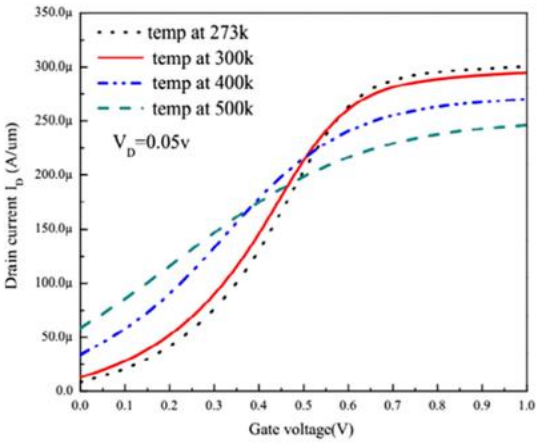

Fig.9. I_D variation at different V_G values by keeping V_D=0.05 volts [25]

- Following observations were made during the course of this study:
  - Increase in gate height degrades **τ**d.
  - Decrease in fin height or fin width or both, improves **τ**d and hence, degrades FoM.

F) "**Temperature-dependent short-channel parameters of FinFETs**" by Rinku Rani Das et al., 2018 [25]

- In this work, various FinFET characteristics were explored and analyzed with respect to varying temperature.

- MuGFET (nanoHUB) simulation software was employed for the simulation purposes.

- Authors of this paper have considered following FinFET characteristics for this study: sub threshold swing, Drain Induced Barrier Lowering (DIBL), threshold voltage and Drain current as a function of temperature.

- Results inferred that in terms of Gate voltage, low temperature performance is more preferable over high temperature.

- On the other hand, in terms of Drain voltage, operating at

- high temperature results in improved performance.

G) "**Analog Performance and Its Variability in Sub-10 nm Fin-Width FinFETs: A Detailed Analysis"** by Mandar S. Bhoir et al., 2019 [26]

- This work studies the effects of sub-10 nm fin width on the analog performance of FinFETs.

- A strong correlation was observed between g_{ds} and DIBL in case of FinFETs with short Gate length which affirms role of DIBL on g_{ds}. Also, DIBL reduced with fin width scaling implying g_{ds} reduction with fin width scaling.

- Degradation of mobility can be decreased by smoothening the fin-side walls.

- g_m degrades and g_{ds} enhances in case of thinner fins leading to less analog performance benefits.

IV. FINFET BASED SRAM CIRCUITS

They offer lower power consumption compared to CMOS for SRAMs. A basic SRAM cell circuit is shown in figure 10.

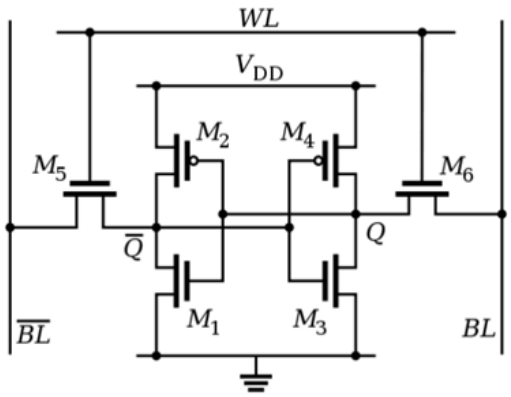

Fig.10. Basic SRAM cell circuit [27]

Table I: SRAM array parameters implemented using FinFET technology

Performance parameters	[28]	[29]	[30]
Length	25 nm	0.355 µm	0.304 µm
Wordline resistance per cell (Ω)	1.02	0.8	3.596
Wordline capacitance per cell (F)	0.58 f	8 f	0.107 f
Bitline resistance per cell (Ω)	0.42	0.73	1.744
Bitline capacitance per cell (F)	0.13 f	2.3 f	0.027 f

Recently, FinFETs have attracted the attention of SRAM (Static Random Access Memory) designers due to the fact that FinFETs have better SCE control and sub threshold slope. We have also compared some research works done on FinFET based SRAM designs based on relevant performance parameters and have summarized them in table I and II.

Table II: Benchmarking of 6T FinFET based SRAM designs

Performance parameters	[27]	[31]	[32]
Transistors	6	6	6
Write delay (ns)	1.95	0.092	0.65
Read delay (ns)	0.47	2.68	2.25
Write Static Noise Margin (V)	0.15	0.401	0.42
Read Static Noise Margin (V)	0.04	0.095	0.135

Owing to the advantages that FinFETs possess, they are being employed by circuit designers for lower technology node implementations. Due to this reason, they are used to design SRAM circuits because memory circuits occupy more than 60 percent of the chip area. So, it is more feasible and advantageous for the designers to employ technology like FinFETs which require lesser area on ICs.

V. CHALLENGES IN FINFETS

1) **Fin dimension variation:** The fin height directly translates to effective width of FinFET structure. It also assumes a very critical role in rendering stability to the whole device. The devices with small fins are more stable as compared to the long fin structures.

2) **Parasitic capacitance:** FinFETs have higher parasitic capacitance as compared to the one present in case of planar MOSFETs. Increase in fin height leads to reduction in gate to fin capacitance [33].

3) **Fin shape:** The fins are designed with an inclination of few degrees with the horizontal axis [34]. This improvisation is carried out with the motive of making FinFET structure robust. But this makes the structure more vulnerable to short channel effects.

4) **Channel doping:** Fully depleted channel is desirable in order to have Gate control over the leakage current, slight doping is done in the channel region. However, this results in damaging the fin structure [35].

5) **Reliability issues:** Due to the continuation of scaling down of FinFETs beyond a certain limit, a concern arises in the areas such as self-heating effect (SHE) and bias temperature instability (BTI) to name a few. BTI can be further classified into two types: positive bias temperature instability and negative bias temperature instability.

6) **Miscellaneous:**

- Layout designing becomes complex for technology node below 28 nm design.

- Number of fabrication-based design rules increase.
- Etching process needs to be highly controlled.
- Printing carried out at technology nodes below 20 nm requires additional masks.

VI. CONCLUSION

FinFETs are emerging out as the next big revolution in the semiconductor industry. In the 1990s, there was a point reached where academicians and researchers doubted whether Moore's law could still stay functional or not. However, the advent of FinFETs eliminated the limitations of planar CMOS transistors and gave a solution in the form of vertical channel transistors. This empowered the designers to make room for more transistors on the same chip area. High packaging density and capability of being operated at low supply voltage proved to be an added benefit. The semiconductor industry has integrated FinFETs in manufacturing integrated circuits customized to provide an edge in power consumption, scalability, performance and enhanced control over channel.

Many promising technologies are coming up as a successor to FinFETs. Gate has a control over the conducting channel from at most three sides in FinFETs but as we progress towards sub-10 nm channel lengths, the electrostatic control again starts reducing. To resolve this issue, semiconductor industry is heading towards devices that provide us Gate control from all the sides such as nanosheet FETs. Some of the other promising alternatives coming up are GAA (Gate All Around) FETs, forksheet FETs, stacked FETs, vertical FETs.

REFERENCES

[1] G. E. Moore and C. I. Corporation, "Cramming more components onto integrated circuits," vol. 38, no. 8, pp. 33–35, 2006.

[2] S. Vidya, A. R. Khan, S. V. Kamat, and V. Venkritesh, "3D FinFET for Next Generation Nano Devices," *Proc. 2018 Int. Conf. Curr. Trends Towar. Converging Technol. ICCTCT 2018*, pp. 1–9, 2018, doi: 10.1109/ICCTCT.2018.8550967.

[3] C. Hu, "Modern semiconductor devices for integrated circuits," *Recherche*, p. 384, 2009, [Online].

[4] S. Borkar, "Design challenges for 22nm CMOS and beyond," *Tech. Dig. - Int. Electron Devices Meet. IEDM*, p. 97124, 2009, doi: 10.1109/IEDM.2009.5424329.

[5] K. J. Kuhn, "Considerations for ultimate CMOS scaling," *IEEE Trans. Electron Devices*, vol. 59, no. 7, pp. 1813–1828, 2012, doi: 10.1109/TED.2012.2193129.

[6] K. Heida et al, "NEW EFFECTS OF TRENCH ISOLATED TRANSISTOR USING SIDE-WALL GATES," pp. 736–740, 1987.

[7] P. Mishra, A. Muttreja, and N. K. Jha, *FinFET circuit design*. 2011.

[8] F. Daugé *et al.*, "Coupling effects and channels separation in FinFETs," *Solid. State. Electron.*, vol. 48, no. 4, pp. 535–542, 2004, doi: 10.1016/j.sse.2003.09.033.

[9] S. S. Amrik Singh, "Evolution of CMOS Technology Past, Present and Future," *Int. J. Eng. Res. Technol.*, vol. 5, no. 2, pp. 304–307, 2016, [Online]. Available: http://www.ijert.org.

[10] M. Bir, S. Gulshan, R. Singh, J. S. Sodhi, and J. S. Sawhney, "Advanced VLSI Technology : FinFET Technology," vol. 6, no. 6, pp. 64–68, 2019.

[11] E. J. N. B. Rainey, D.M. Fried, M. Leong, J. Kedzierski, "Demonstration of FinFET CMOS circuit," vol. 437440, pp. 47–48, 2001.

[12] I. F. et al. N. Collaert, M. Demand, "Tall triple-gate devices with TiN/HfO2 gate stack," *J. Chem. Inf. Model.*, vol. 12 Suppl 1, no. 9, pp. 1–29, 2005, [Online].

[13] H. Lee *et al.*, "Sub-5nm all-around gate FinFET for ultimate scaling," *Dig. Tech. Pap. - Symp. VLSI Technol.*, vol. 25, no. 9, pp. 58–59, 2006, doi: 10.1109/vlsit.2006.1705215.

[14] Y. Taur and T. H. Ning, "Fundamentals of Modern VLSI Devices," *Cambridge Univ. Press*, p. 310, 2013, [Online].

[15] C. Hu, "Gate oxide scaling limits and projection," *Tech. Dig. - Int. Electron Devices Meet.*, pp. 319–322, 1996, doi: 10.1109/iedm.1996.553593.

[16] M. Poljak, V. Jovanović, and T. Suligoj, "Improving bulk FinFET DC performance in comparison to SOI FinFET," *Microelectron. Eng.*, vol. 86, no. 10, pp. 2078–2085, 2009, doi: 10.1016/j.mee.2009.01.066.

[17] L. Yuxi and X. Qiang, "On modeling faults in FinFET logic circuits BT - Test Conference (ITC), 2012 IEEE International," pp. 1–9, 2012.

[18] M. Manorama, P. Shrivastava, S. Khandelwal, and S. Akashe, "Threshold Voltage Control through Multiple Supply for Low Power IG-FinFET Circuit," *Int. J. Comput. Appl.*, vol. 78, no. 8, pp. 11–15, 2013, doi: 10.5120/13508-1261.

[19] A. Goel and N. R. Prakash, "The Effect of Doping on Different FET Structures: MOSFET, TFET and FinFET," *Int. J. Innov. Technol. Explor. Eng.*, vol. 9, no. 6, pp. 972–979, 2020, doi: 10.35940/ijitee.f4051.049620.

[20] M. O. Simsir, A. Bhoj, and N. K. Jha, "Fault modeling for FinFET circuits," *Proc. 2010 IEEE/ACM Int. Symp. Nanoscale Archit. NANOARCH 2010*, pp. 41–46, 2010, doi: 10.1109/NANOARCH.2010.5510927.

[21] G. Harutyunyan, G. Tshagharyan, and Y. Zorian, "Impact of parameter variations on FinFET faults," *Proc. IEEE VLSI Test Symp.*, vol. 2015-Janua, pp. 6–9, 2015, doi: 10.1109/VTS.2015.7116276.

[22] N. Somra and R. Singh Sawhney, "32 nm Gate Length FinFET: Impact of Doping," *Int. J. Comput. Appl.*, vol. 122, no. 6, pp. 11–14, 2015, doi: 10.5120/21703-4816.

[23] M. S. Badran, H. H. Issa, S. M. Eisa, and H. F. Ragai, "Low Leakage Current Symmetrical Dual-k 7 nm Trigate Bulk Underlap FinFET for Ultra Low Power Applications," *IEEE Access*, vol. 7,

pp. 17256–17262, 2019, doi: 10.1109/ACCESS.2019.2895057.

[24] J. Jeon, H. S. Jhon, and M. Kang, "Investigation of Electrothermal Behaviors of 5-nm Bulk FinFET," *IEEE Trans. Electron Devices*, vol. 64, no. 12, pp. 5284–5287, 2017, doi: 10.1109/TED.2017.2766214.

[25] R. R. Das, S. Maity, A. Choudhury, A. Chakraborty, C. T. Bhunia, and P. P. Sahu, "Temperature-dependent short-channel parameters of FinFETs," *J. Comput. Electron.*, vol. 17, no. 3, pp. 1001–1012, 2018, doi: 10.1007/s10825-018-1212-y.

[26] M. S. Bhoir *et al.*, "Analog Performance and its Variability in Sub-10 nm Fin-Width FinFETs: A Detailed Analysis," *IEEE J. Electron Devices Soc.*, vol. 7, no. Xx, pp. 1217–1224, 2019, doi: 10.1109/JEDS.2019.2934575.

[27] D. Vaithiyanathan, M. B. Raj, S. E. P. Pushpa, and R. Seetharaman, "Performance analysis of FinFET and negative capacitance FET over 6T SRAM," *IEEE Int. Conf. Circuits Syst. ICCS 2017*, vol. 2018-Janua, no. Iccs, pp. 196–201, 2018, doi: 10.1109/ICCS1.2017.8325989.

[28] H. Ananthan, A. Bansal, and K. Roy, "Finfet sram - Device and circuit design considerations," *Proc. - 5th Int. Symp. Qual. Electron. Des. ISQUED 2004*, pp. 511–516, 2004, doi: 10.1109/ISQED.2004.1283724.

[29] A. Bansal, S. Mukhopadhyay, and K. Roy, "Device-optimization technique for robust and low-power FinFET SRAM design in NanoScale era," *IEEE Trans. Electron Devices*, vol. 54, no. 6, pp. 1409–1419, 2007, doi: 10.1109/TED.2007.895879.

[30] B. Ebrahimi, S. Zeinolabedmzadeh, and A. Afzali-Kusha, "Low standby power and robust FinFET based SRAM design," *Proc. - IEEE Comput. Soc. Annu. Symp. VLSI Trends VLSI Technol. Des. ISVLSI 2008*, no. April, pp. 185–190, 2008, doi: 10.1109/ISVLSI.2008.8.

[31] M. U. Mohammed, A. Nizam, and M. H. Chowdhury, "Performance stability analysis of SRAM cells based on different FinFET devices in 7nm technology," *2018 IEEE SOI-3D-Subthreshold Microelectron. Technol. Unified Conf. S3S 2018*, pp. 1–3, 2019, doi: 10.1109/S3S.2018.8640161.

[32] M. U. Mohammed, A. Nizam, and M. H. Chowdhury, "Performance and Reliability of Asymmetrical Underlapped FinFET based 6T and 8T SRAMs in Sub-10nm Domain," *2018 IEEE Nanotechnol. Symp. ANTS 2018*, pp. 1–4, 2019, doi: 10.1109/NANOTECH.2018.8653566.

[33] W. P. Maszara and M. R. Lin, "FinFETs - Technology and circuit design challenges," *Eur. Solid-State Device Res. Conf.*, pp. 3–8, 2013, doi: 10.1109/ESSDERC.2013.6818808.

[34] Y. Li and C. Hwang, "Effect of Fin Angle on Electrical Characteristics of," *IEEE Trans. IEDM*, vol. 54, no. 12, pp. 3426–3429, 2007.

[35] J. P. Colinge and A. Chandrakasan, *FinFETs and other multi-gate transistors*. 2008.

AUTHORS

First Author – Mohit Shukla, MTech Microelectronics, Institute of Engineering and Technology, Lucknow.

Second Author – Pawan Srivastava, MTech Microelectronics, Institute of Engineering and Technology, Lucknow.

Third Author – Ram Chandra Singh Chauhan, Associate Professor, Electronics and Communication Engineering Department, Institute of Engineering and Technology, Lucknow.s

Correspondence Author – Mohit Shukla, Email:1900521195003@ietlucknow.ac.in