

A Review On Carbon Nanotubes And Comparative Study Of VCO Circuits Based On CNTFET Technology

Pawan Srivastava*, Mohit Shukla*, Ram Chandra Singh Chauhan**

* M. Tech. Microelectronics, Institute of Engineering and Technology, Lucknow, India -226021.

** Associate Professor, ECE Department, Institute of Engineering and Technology, Lucknow, India -226021.

Abstract- Since the MOSFET transistors can be scaled down too much smaller dimension for that reason the CMOS technology encountered vast growth over the years. But further scaling in deep nanometer regime gives rise to limitations like short channel effect, large leakage currents and high-power dissipation. These drawbacks can be reduced by using the Carbon Nanotube as the channel material. In this paper, the review of CNTFET is carried out. The study of carbon nanotube and different types of CNTFET are done. Also, study of carbon nanotube field effect transistor based ring Voltage Controlled Oscillator is done, and performance comparison is shown. It can be used in various applications like bio-sensing, RF applications, electrical applications, and logic and storage devices due to its low power consumption, higher mobility and high temperature resilience.

Index Terms- Carbon nanotube, CNTFET, Short channel effect, VCO, Scaling.

I. INTRODUCTION

According to Moore's law, the transistor numbers are increasing exponentially. So, there is requirement of diminishing the size of transistor i.e., reducing the dimension of MOSFET. CMOS technology based upon MOS shows a continuous growth in this due to enhancement in circuit speed and low power dissipation.

But when transistors are scaled down in nanometer scale (below 22nm) CMOS technology finds difficulty in this due to short channel effects. Increased power dissipation and high leakage current [1] is other major concern of MOSFET. The solution to overcome this problem is by use of new material in place of Si MOSFET. The channel is off carbon nanotube in (CNTFET) is an ideal replacement. Carbon nanotubes are allotropes of carbon with diameters measured in nanometers and having high current density, ultra-light weight and quasi 1-D ballistic transport of electron and holes. This paper is as follows: Section 2 gives the brief description of Carbon Nanotube. Section 3 elucidate the CNTFET and its classification. Section 4 explains CNTFET based VCO and its comparison. Section 5 is the challenges in CNTFETs, and Section 6 is the conclusion.

II. CARBON NANOTUBE

Carbon nanotube (CNTs) was first discovered by Sumio Iijima in 1991. They are formed by rolling the sheet of graphene and shape is like a hollow cylinder. CNTs are of two types: Single walled and Multi-walled. Single walled carbon nanotube (SWCNT) is made by wrapping up of single sheet of graphene. The catalytic material like Fe or Co when combined with carbon source at high temperature, SWCNT is grown [2].

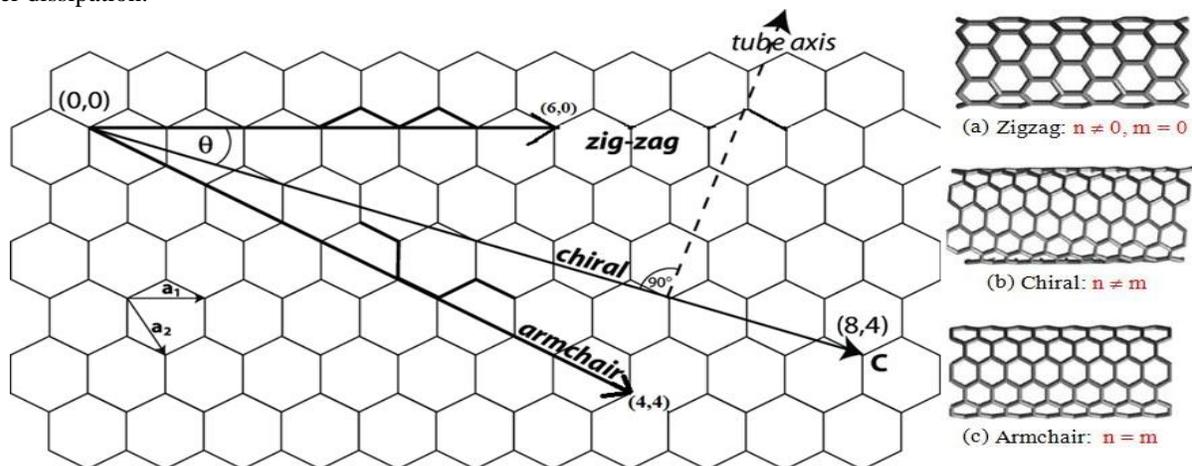


Figure 1. Geometry of carbon nanotube and its different configurations

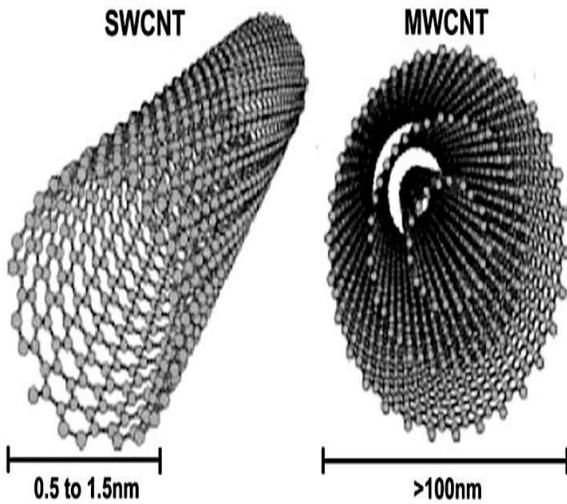


Figure 2. Single walled and Multi walled carbon nanotube [5]

SWCNT have a mean diameter of 0.4nm -4nm. Multi walled carbon nanotube (MWCNT) made up of several coaxial shells of carbon with diameter of about several nm to 100nm. MWCNT can be called as metallic conductors and its fabrication is simpler than SWCNT [3]. MWCNT is difficult to model than SWCNT because it has a complex structure [3]. SWCNT can be semiconductors or metals depending upon its chirality.

The chiral vector C pointed from one atom to second atom is given by the relation [4]

$$C = n a_1 + m a_2 \tag{1}$$

Armchair, chiral and zigzag are the three ways by which graphene sheet is rolled.

If $n=m$; armchair and shows metallic nature, $n \neq m$ chiral (general) and if $n \neq 0, m=0$ then zigzag exhibit both nature; metallic (if $n-m$ is a multiple of 3) else semiconducting. The diameter for SWCNT with chirality (m, n) is given by [6] [7]

$$D = \frac{\sqrt{3}a_0}{\pi} \sqrt{n^2 + m^2 + mn} \tag{2}$$

Where a_0 is interatomic distance between two adjacent carbon atoms and $a_0 = 0.142nm$.

III. CNTFET AND ITS TYPES

CNTFETs were first illustrated in the year 1998 [8]. The working principle of CNTFET is alike MOSFET only the channel is off carbon nanotube. Carbon nanotubes composed of sp^2 bonds same as in graphite. The reason behind using CNTFETs is their 1-D characteristic and its ability to change its threshold voltage by selecting various diameter of carbon

nanotube. The operation is like MOSFET and its threshold voltage is the minimum voltage at which gate starts conducting. The threshold voltage can be calculated by the formula [11]

$$V_{th} \approx \frac{E_G}{2e} = \frac{\sqrt{3} a V_{\pi}}{3 e D} \approx \frac{0.436}{D} \tag{3}$$

Where e is charge of electron, E_G represent the energy band gap, $a=2.49 \text{ \AA}$, $V_{\pi}=3.033 \text{ eV}$ is the $\pi - \pi$ bond energy of carbon atom. Thus, by changing D value the threshold voltage can also be varied. CNTFET can be classified into various types depending upon its geometry and operation.

A Based on Geometry:

i) Back gated CNTFET:

It was first presented in 1998 [8]. Here, SWCNT placed on Si wafer with oxidised outermost layer. On the nanotube drain and source electrodes were kept. Highly doped Si substrate itself acts as back gate. Its operation is similar to p-type FETs with high I_{on}/I_{off} ratio and high parasitic capacitance [10]. Figure 3 shows the back gate CNTFET. The drain voltage is fixed hence drain gate depends highly on gate voltage and causes gain.

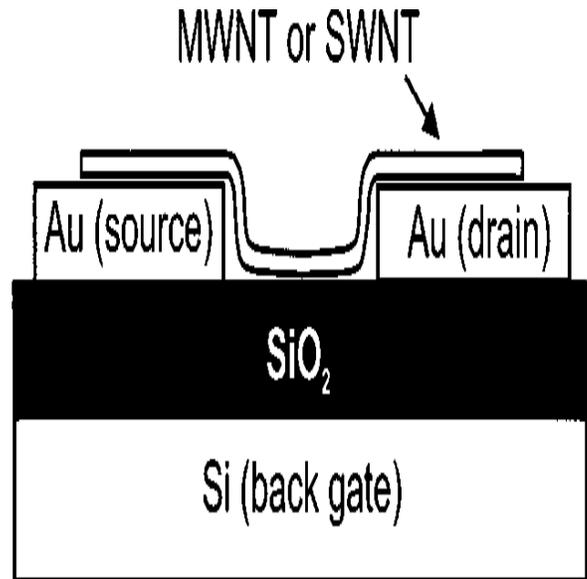


Figure 3. Back-gate CNTFET [9]

ii) Top -gated CNTFET

To improve device performance, the next type of CNTFET is introduced known as top gated CNTFET in 2003 [12]. Figure 4 shows the schematic in which Ti used as source, drain electrodes. Silicon dioxide film used as gate oxide. The gate dielectric is placed over the carbon nanotube. Here, atomic force microscopy (AFM) is used to track down the individual carbon nanotube. It has higher transconductance, less

threshold voltage required and higher I_{on}/I_{off} ratio than back gate CNTFET [10].

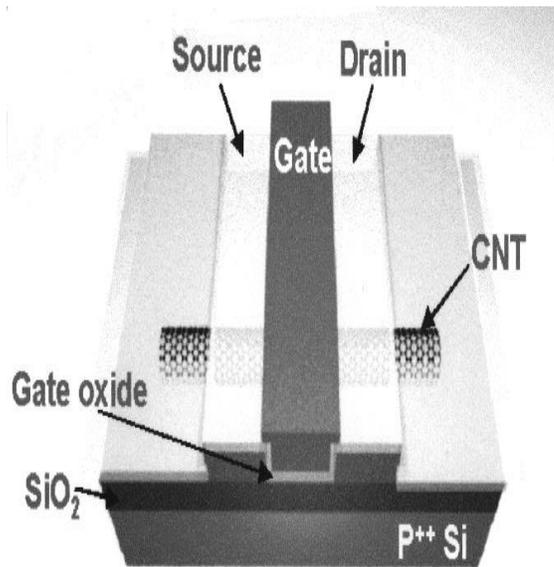


Figure 4. Top-gate CNTFET Structure [10]

iii) Wrap around CNTFET

It is also known as the gate all around CNTFET. The structure of wrap around CNTFET is better than the top gate device. In this entire circumference of nanotube is gated. Figure 5 shows the wrap around gate CNTFET. This causes reduction in leakage current and improves electrical characteristics. It was formed by wrapping CNTs in a gate dielectric via atomic layer deposition and the nanotube are etched where drain and source are adhered.

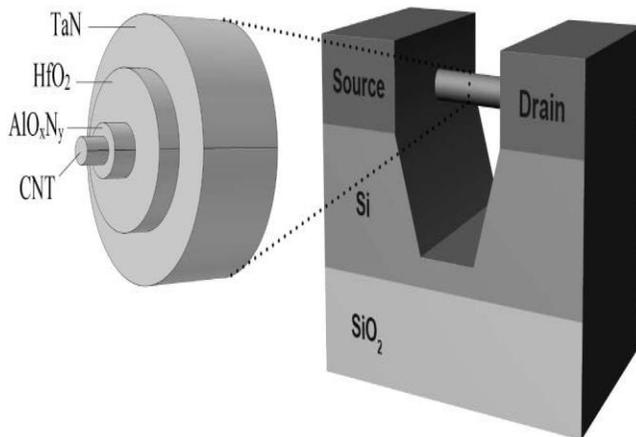


Figure 5. Wrap-gate CNTFET structure [13]

B Based on Operation:

i) Schottky barrier CNTFET

In this, the channel region consists of intrinsic CNT and is connected to metal i.e., Source and drain to form Schottky barriers at the junctions. Al, Ti, Pd are the materials used for metals. The transistor action occurs by changing the contact resistance. Schottky barrier CNTFETs are highly ambipolar in nature [15]. In source channel junction direct tunneling is done. Its limitation is that the barrier height is estimated by the filling of metal-induced gap states. These states cause increase in source to drain tunneling due to decrease in channel length [17].

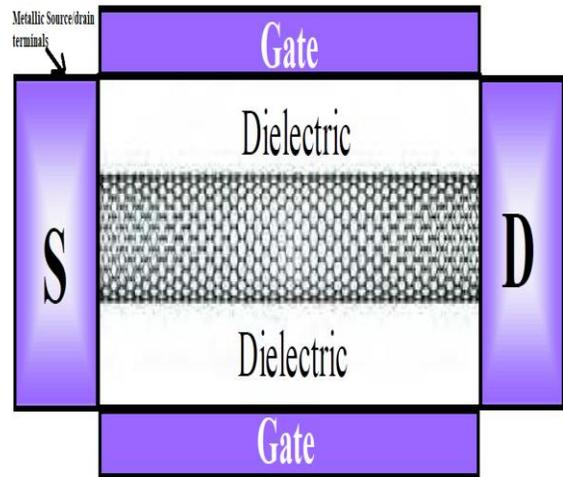


Figure 6: Schottky barrier CNTFET with metallic source/drain [16]

ii) MOSFET like CNTFET

The structure of MOSFET like CNTFET uses heavily doped terminals instead of metal thus its structure is different from Schottky barrier one. It overcomes limitations of ambipolar behavior in SB-CNTFET by operating like normal MOSFET.

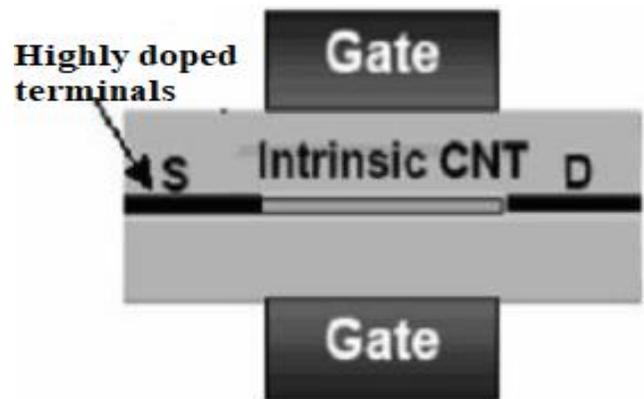


Figure 7: MOSFET like CNTFET structure [20]

Here, the gate voltage controls current intensity in the transistor channel. High speed operation can be achieved since length between gate and source/drain terminals can be separated by the length [17]. This device is obvious choice for the ballistic transport in CNTFET.

iii) Tunneling based CNTFET

Band to band tunneling is a phenomenon by means of which electrons can tunnel from conduction band via semiconductor band gap to valence band and inverse is also correct [19]. In tunnel CNTFET, source and drain are heavy doped and of opposite type (i.e. p^+ and n^+) and channel is of intrinsic CNT. Here, tunneling takes place in drain and source metal contacts. Its disadvantage is dependency of current on tunneling of electron and holes which is not as much compared to other CNTFET thus it is fitting for low energy devices.

IV CNTFET BASE RING VCO

Ring oscillator is basically formed by connecting odd number of inverters where output of last inverter is connected to input of first inverter. Figure 8 shows a 5 stage ring oscillator made up of single wall p-type CNTFET and n-type CNTFET [25].

There is various ring based VCO like current starved VCO, delay stage ring VCO are used because of advantages of lower power consumption and wider tuning range. CNTFET based VCO works similar as CMOS based VCO with more improved power consumption, oscillation frequency and lesser phase noise.

The oscillation frequency is given as

$$f_o = \frac{1}{2NT} \quad (4)$$

Where N=inverter stages, T=propagation delay of each inverter.

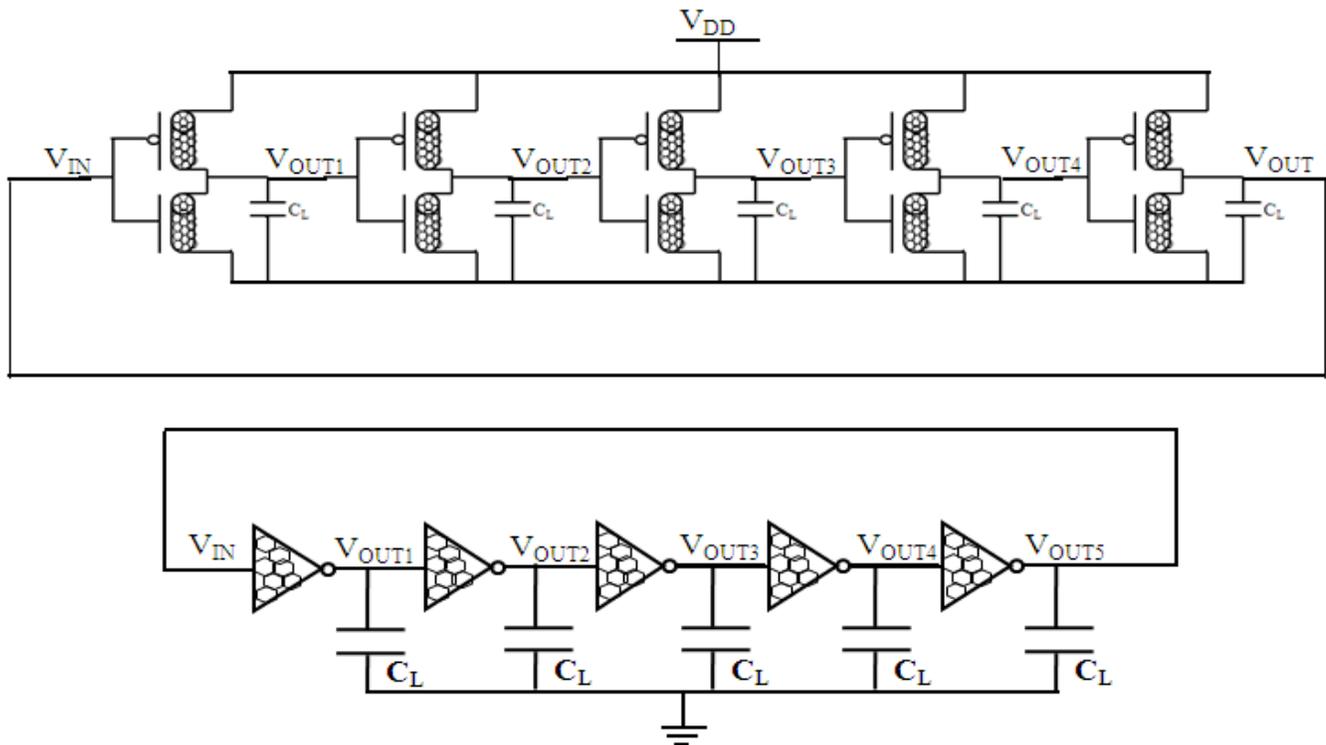


Figure 8. CNTFET based ring oscillator [25]

The performance comparisons of various ring based VCOs are shown in table 1. From the table shown above, it was found that pure CNTFET based VCO [27] consumes lesser power but its frequency is smaller than other VCOs while the GAA-CNTFET VCO [28], [26] gives overall better performance than other VCOs designs.

V Challenges in CNTFET

CNTFETs have been proposed as a promising technology to replace the traditional CMOS technology. But this technology faces serious challenges. Some of them are discussed below:

- 1) The fabrication of billions of carbon nanotubes must be done at certain positions on IC chip. They should possess the similar electronic properties. This kind of mass production of CNTFETs along with the lower cost are difficult to achieve.

VCOs	GAA-CNTFET [26]	TG-CNTFET [26]	Pure-CNTFET [27]	GAA-CNTFET [28]	TG-CNTFET [29]	Hybrid CMOS-CNTFET [30]
Supply Voltage	0.9	0.9	0.9	0.8	1	0.8
Power Consumption (μ W)	85.17	85.67	0.372	6.011	542	65.4
Oscillation Frequency (GHz)	6.36	6.23	$150 * 10^{-4}$	1.205	9	1.6
Phase Noise dBc/Hz @ 1MHz offset	-90.747	-89.19	NA	-91.6	-66	NA

Table 1. Performance comparison between various CNTFET-based ring VCOs

- 2) Scalability of CNTFETs is a very different technological challenge to overcome.
- 3) CNTFETs have reliability issues because at high electric fields leads to problem of temperature gradient.
- 4) CNTFETs gets degraded when exposed to oxygen.
- 5) Development of passivation techniques for Carbon nanotubes are needed.

VI CONCLUSION

The progression of carbon nanotube transistors over the past few decades has made CNTFET technology ideal to replace Si based CMOS technology. In this paper, carbon nanotube and its types are studied in brief. Also, CNTFET based ring oscillator is reviewed and performance comparison is done. CNTFET technology has the potential to go below 7nm technology. The various types of CNTFETs are considered and found out that they provide high performance with low power consumption than conventional CMOS. CNTFETs uses innovative design techniques to improve the circuit parameters thus they are used as an alternative for FinFETs and CMOS technology.

REFERENCES

- [1] D. J. Frank et al., "Device scaling limits of Si MOSFETs and their application dependencies," in Proceedings of the IEEE, vol. 89, no. 3, pp. 259-288, 2001. doi: 10.1109/5.915374.
- [2] P. L. McEuen et al., "Single-walled carbon nanotube electronics," in IEEE Transactions on Nanotechnology, vol. 1, no.1, pp.78-85, 2002. doi:10.1109/TNANO.2002.1005429.
- [3] H. Li, W.-Y. Yin, K. Banerjee, & J.-F. Mao, "Circuit Modeling and Performance Analysis of Multi-Walled Carbon Nanotube Interconnects," IEEE Trans. on Electron Devices, 55(6), 1328-1337, 2008. doi:10.1109/ted.2008.922855.
- [4] M. S. Dresselhaus, G. Dresselhaus, & R. Saito, "Physics of carbon nanotubes". Carbon, 33(7), 883-891, 1995.
- [5] M. Scarselli, P. Castrucci, & M. De Crescenzi, "Electronic and optoelectronic nano-devices based on carbon nanotubes". Journal of Physics: Condensed Matter, 24(31), 313202, 2012. doi:10.1088/0953-8984/24/31/313202.
- [6] J. Deng, & H.-S. P. Wong, "A Compact SPICE Model for Carbon-Nanotube Field-Effect Transistors Including Non-idealities and Its Application—Part I: Model of the Intrinsic Channel Region". IEEE Transactions on Electron Devices, 54(12), 3186-3194, 2007. doi:10.1109/ted.2007.909030
- [7] S. Lin, Y.-B. Kim, & F. Lombardi, "CNTFET-Based Design of Ternary Logic Gates and Arithmetic Circuits" IEEE Transactions on Nanotechnology, 10(2), 217-225, 2011.
- [8] S. J. Tans, R. M. Verschueren Alwin and C. Dekker, "Room-temperature transistor based on a single carbon nanotube". Nature Vol.393, pp. 49-52, 1998.
- [9] R. Martel et al., "Single- and multi-wall carbon nanotube field-effect transistors" Applied Physics Letters, 73(17), 2447-2449, 1998. doi:10.1063/1.122477.
- [10] P. Avouris, J. Appenzeller, R. Martel and S. J. Wind, "Carbon nanotube electronics," in Proceedings of the IEEE, vol. 91, no. 11, pp. 1772-1784, Nov, 2003. doi: 10.1109/JPROC.2003.818338.
- [11] H. Samadi, A. Shahhoseini, F. Aghaei-liavali, "A new method on designing and simulating CNTFET based ternary gates and arithmetic circuits". Microelectron. J. 2017, 63, 41-48, 2017.
- [12] S. J. Wind, J. Appenzeller & P. Avouris, "Lateral Scaling in CNTFET Transistors" Physical Review Letters, 91(5), 2003.
- [13] V. Dokania et al., "Analytical Modeling of Wrap-Gate Carbon Nanotube FET with Parasitic Capacitances and Density of States". IEEE Trans. on Electron Devices, 63(8), 2016.
- [14] R. Hajare et al., "Performance enhancement of FINFET and CNTFET at different node technologies. Microsystem Technologies", 22(5), 1121-1126, 2015. doi:10.1007/s00542-015-2468-9.
- [15] S. Heinze et al., "Carbon Nanotubes as Schottky Barrier Transistors" Physical Review Letters, 89(10), 2002.
- [16] Z. Kordrostami, & M. Hossein, "Fundamental Physical Aspects of Carbon Nanotube Transistors" Carbon Nanotubes, 2010. doi:10.5772/39424.
- [17] D. L. John et al., "Electrostatics of coaxial Schottky-barrier nanotube field-effect transistors" IEEE Transactions on Nanotechnology, 2(3), 175-180, 2003. doi:10.1109/tnano.2003.817228.

- [18] B. C. Devnath and S. N. Biswas, "MOSFET-like CNTFET based Full adder design," 1st International Conference on Advances in Science, Engineering and Robotics Technology (ICASERT), 2019. doi: 10.1109/ICASERT.2019.8934521.
- [19] A. D. Es-Sakhi, & M. H. Chowdhury, "Multichannel Tunneling Carbon Nanotube Field Effect Transistor (MT-CNTFET)" 27th IEEE International System-on-Chip Conference (SOCC), 2014. doi:10.1109/socc.2014.6948918.
- [20] M. Fedawy et al. , "I-V characteristics model for ballistic Single Wall Carbon Nanotube Field Effect Transistors (SW-CNTFET)," IEEE International Conference on Electronics Design, Systems and Applications (ICEDSA), 2012, pp. 10-13, doi: 10.1109/ICEDSA.2012.6507775.
- [21] N.Valed Karimi, & Y.Pourasad, "Investigating the effect of some parameters of the channel on the characteristics of tunneling carbon nanotube field-effect transistor". International Nano Letters, 6(4), 215–221, 2016. doi:10.1007/s40089-016-0182-y
- [22] A. Eapen Chacko et al., "Performance analysis of Carbon Nanotube Field Effect Transistor with high K dielectric," International Conference on Electronics and Communication Systems (ICECS), Coimbatore, 2014, pp. 1-4, doi: 10.1109/ECS.2014.6892700.
- [23] Rasmita Sahoo and R. R. Mishra , "Simulations of CNTFETs ", International Journal of Electronic Engineering Research ISSN 0975-6450 Volume.1 Number 2 pp. 117–125, 2009.
- [24] Amandeep Singh, & Mamta Khosla & Balwinder. Raj, "Comparative Analysis of Carbon Nanotube Field Effect Transistor and Nanowire Transistor for Low Power Circuit Design" Journal of Nanoelectronics and Optoelectronics. 11, . 388-393, 2016.
- [25] Lobna Imsaddak et al., "Low Power of Ring Oscillator Based on CNTFET". IJCSI, Vol. 10, Issue 3, No 2, 2013.
- [26] Mohammad Khaleqi et al. , "A low-power delay stage ring VCO based on wrap-gate CNTFET technology for X-band satellite communication applications". Int. Journal of Circuit Theory and Applications. 49. 1-17, 2020.
- [27] Pramod R.Gunjal , Sandip B.Rahane, "Performance Analysis of Current Starved Voltage Controlled Oscillator". IJMETR Vol No.2 Issue6, 2015.
- [28] Mohammad Khaleqi et al., "Design and Performance Analysis of Wrap-Gate CNTFET-Based Ring Oscillators for IoT Applications", 2019.
- [29] Y Kumar et al., "High-frequency CNTFET-based voltage-controlled oscillator for PLL application". Micro-Electronics and Telecommunication Engineering. Singapore: Springer;413-419, 2020.
- [30] Sandip Rahane & A.K.Kureshi, "A low power and linear voltage controlled oscillator using hybrid CMOS-CNFET technology". International Journal of Applied Engineering Research. 12. 1969-1973, 2017.

AUTHORS

First Author – Pawan Srivastava , MTech Microelectronics, Institute of Engineering and Technology, Lucknow.

Second Author – Mohit Shukla , MTech Microelectronics, Institute of Engineering and Technology, Lucknow.

Third Author – Ram Chandra Singh Chauhan, Associate Professor, Electronics and Communication Engineering Department, Institute of Engineering and Technology, Lucknow.

Correspondence Author – Pawan Srivastava ,
Email: 1900521195005@ietlucknow.ac.in